Final Project: IEEE 8500 Node Test Feeder

EE 558 Winter 2015

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1 Executive Summary

The IEEE 8500 Node Test Feeder was examined across three 24–hour time periods, two in the summer and one in the winter. During the winter time period, regulators were found to tap change too often, capacitors were not being used at all, and numerous houses were found to be falling below ANSI Voltage Standard minimums.

Analysis of the model with GridLAB–D and incremental adjustments reduced regulator tap changes to more reasonable limits (fewer than 24 tap changes per phase per day), utilized capacitor banks, and eliminated all ANSI Voltage Standard minimum violations. Some ANSI Voltage Standard maximums were exceeded.

2 Introduction

An initial simulation of the model was done without making any modifications to the regulator and capacitor settings. Numerous problems were found. As can be seen in Figure 1 and Table 1, three of the four regulators were tap changing over 100 times per phase per day. Effective regulator use is tap changing fewer than 24 times per day. This is because each tap change costs around $0.05. Tap changing 100 times per day means the regulator will wear out faster and need replaced often. Also, when the regulator changes taps quickly back and forth between two points, there is no benefit gained for the end user.

Although capacitor banks were installed on the system and were capable of switching on and off during the day, they were not switching at all. Capacitors could be used to decrease current and thus reduce voltage drop. They could be used to improve regulator effectiveness.

And perhaps the most glaring problem, 161 consumers were experiencing voltage levels lower than the ANSI Voltage Standard requirement. A voltage profile for the winter day showing two legs of the system can be seen in Figure 2. Given that the voltage had already fallen below standards at VREG3, it is clear that the voltage at numerous end nodes would violate ANSI minimum voltage standards.

In addition to the problems that need addressed to bring the utility better use of its equipment and into code with ANSI Voltage Standards, the model had some questionable simulation settings. Some capacitors were set to use remote sensing for elements very far away from themselves and most elements were using time delays far too short. This means they would more closely match the system but it also means, for regulators, that they would tap change too often. The zoomed in view shown in Figure 3 demonstrates the the voltage is going up and down over 200 volts every five minutes. The voltage range covered is greater than a tap change and the time delay on regulators, set at only 120 seconds, meant they were tap changing several times per rise and fall.

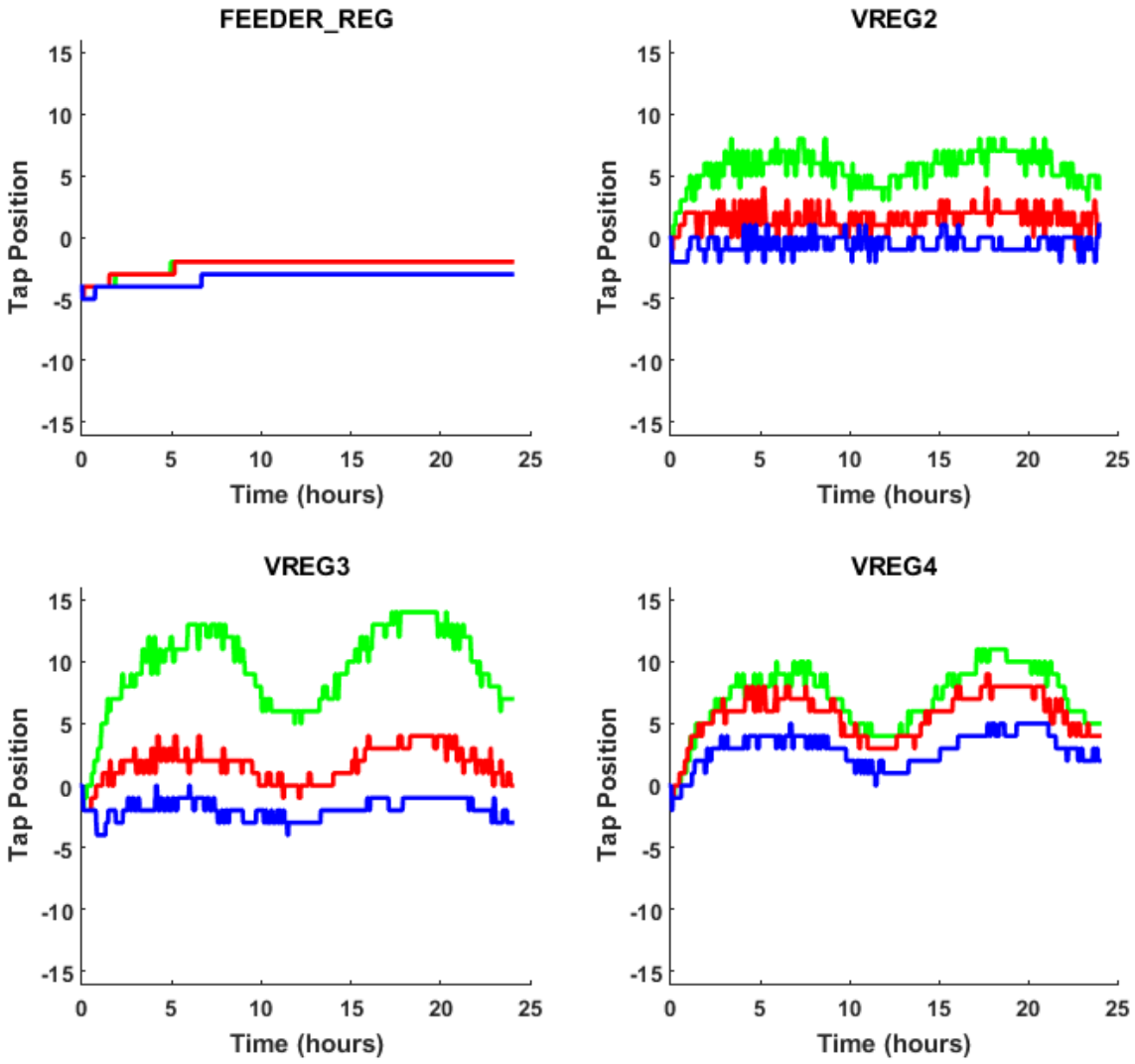

Figure 1: Plots showing regulator tap changes per phase for the winter day of January 11, 2014. Green is Phase A, Red is Phase B, and Blue is Phase C. Tap change totals per phase for these plots are shown in Table 1.

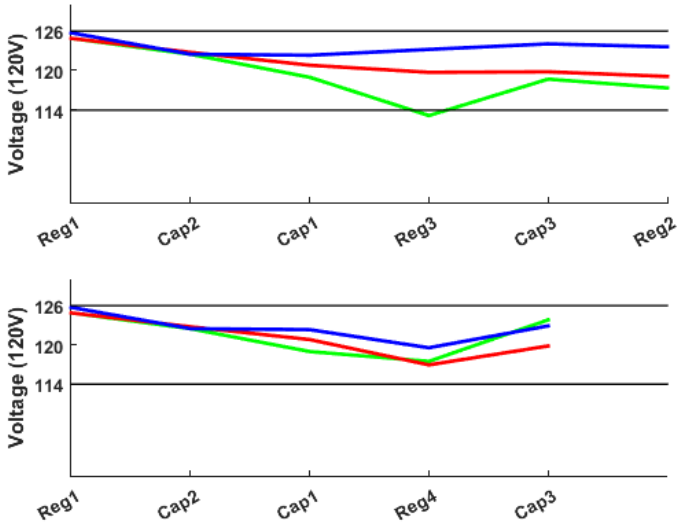

Figure 2: Initial voltage profile of the system showing voltage levels on to upper (top) and lower (bottom) legs of the feeder.

	FEEDER_REG	**VERG2**	**VREG3**	**VREG4**
Phase A Tap Total	2	206	135	101
Phase B Tap Total	4	209	112	90
Phase C Tap Total	3	139	71	76

Table 1: Total tap counts per regulator per phase for the initial configuration during the winter day of January 11, 2014.

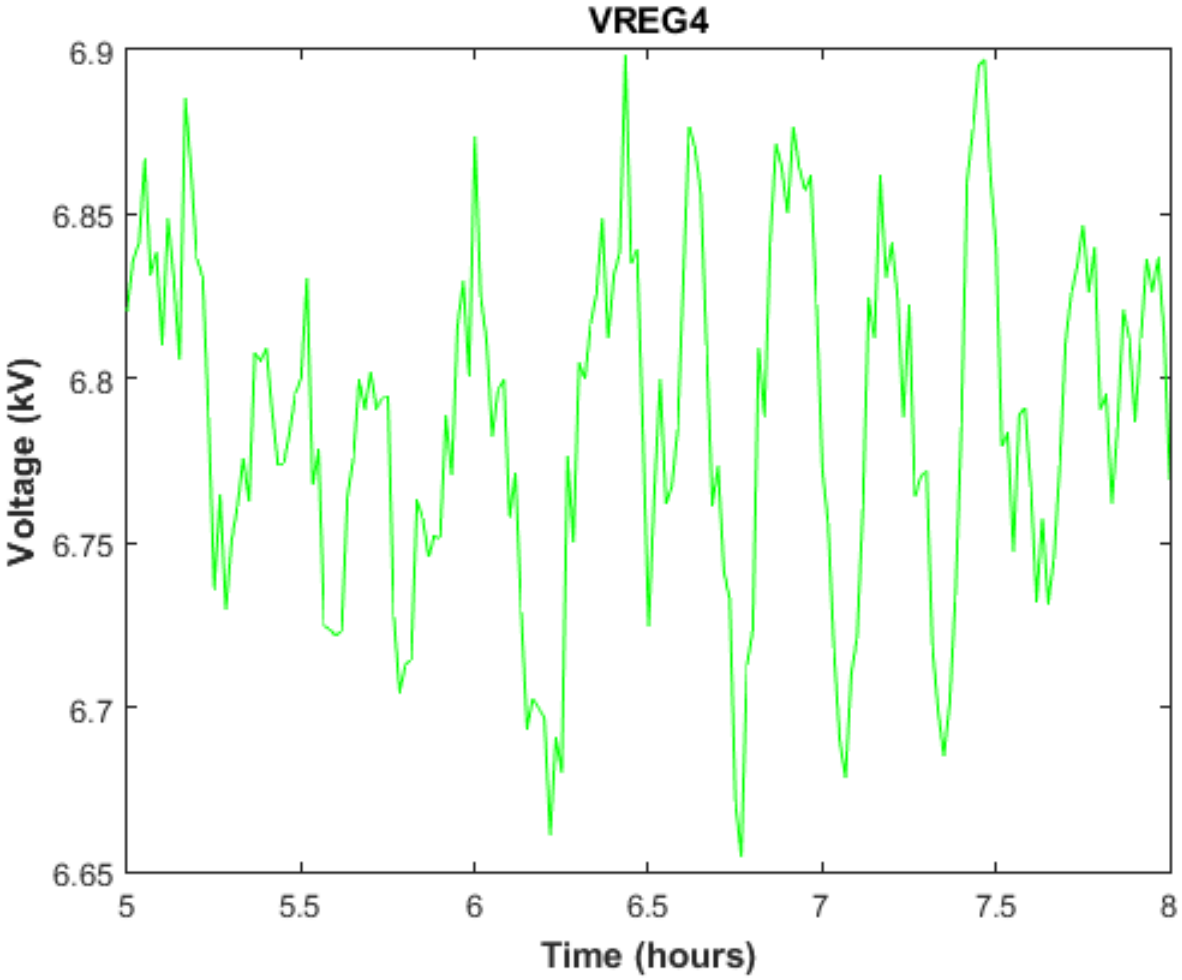

Figure 3: A zoomed in segment of VREG4's voltage during a January 11, 2014 simulation. The maximum peak to peak distance in this segment is 243V.

2.1 Model Information

The IEEE 8500 Node Test Feeder is a model designed by the IEEE Power & Energy Society's (PES) Test Feeders Working Group (WG) of the Distribution System Analysis (DSA) Subcommittee of the Power Systems Analysis, Computer, and Economics (PSACE) Committee[1]. This particular test feeder is more extensive than most available feeders. It was designed by using a real system and adding various other scenarios to it. It is a radial distribution feeder. A map of the feeder was provided in the PES documentation on the 8500 Node Test Feeder, a copy of which is shown in Figure 4.

The original design of the feeder calls for a static analysis at a heavily loaded point in time. This project takes the model one step further by doing a time series analysis. Although solving a system for peak load can be effective, it ignores the problems that such a solution might cause for other periods when the load is not so high. It also ignores possible chain–reactions that can occur with regulator tap changing and capacitor switching.

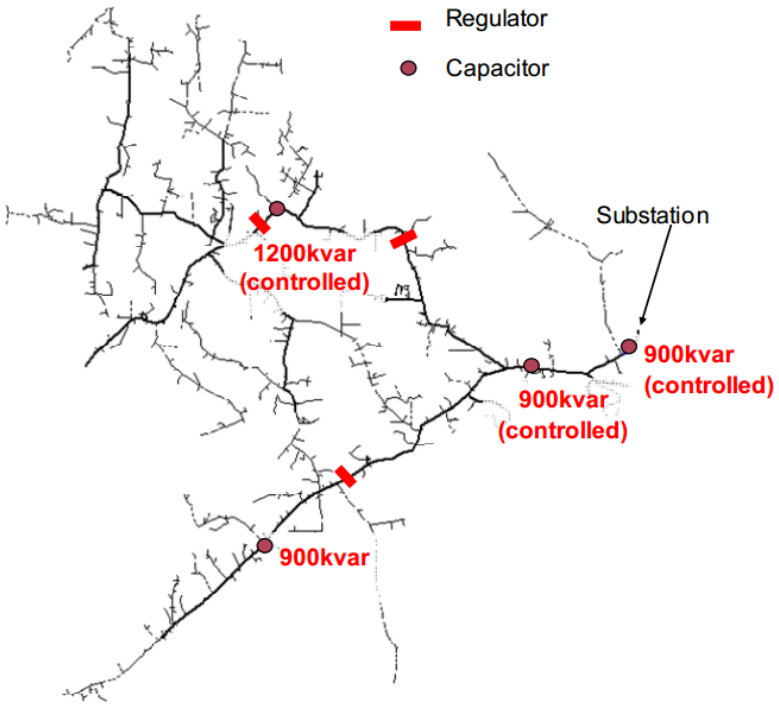

Figure 4: A one-line diagram of the IEEE 8500 Node Test Feeder circuit.[1]

2.2 Time–Series Load Data

The data for the 8500 Node Test Feeder comes in a set of CSV files. Fortunately, a copy of the model was provided already created in GridLAB–D. GridLAB–D is an open–source distribution system analysis product developed by the US Department of Energy (DOE) at Pacific Northwest National Laboratory (PNNL)[2].

By default, the 8500 Node Test Feeder comes with a peak–load condition only. For this class, the model came pre–configured with time–series load data. For the purposes of this project, three different 24–hour simulations are run:

- Saturday, January 11, 2014
- Friday, August 8, 2014
- Sunday, August 10, 2014

2.3 Analysis Goals

The settings for capacitors and regulators within the model are optimized to reduce tap changing and utilize capacitor switching while keeping all metered nodes within ANSI Standard voltages across all three time periods. Optimal targets follow:

- Optimal Regulator tap changing is assumed to be fewer than 24 tap changes per phase per day.
- Optimal Capacitor switching is assumed to be fewer than 6 switches per phase per day.
- Meter node voltages are considered optimal when ANSI Standards are met for on every single node at the peak power demand. Peak power demand means highest current which produces the largest voltage drop over the length of the system.

3 Methods

A combination of GridLAB–D and Matlab was used to analyze the model. GridLAB–D was used to run simulations and record data while Matlab was used to analyze recorded data and generate plots. Ruby scripts were employed to generate GridLAB–D voltdump glm files. Matlab scripts were written to streamline the parsing and visualization of data recorded by GridLAB–D.

3.1 Regulator Settings

Regulators are used to maintain a constant reasonable voltage at a location. In GridLAB–D, regulators are point objects. There is a *regulator_configuration* object available with options to control regulators. Regulator properties for this project are limited to the those shown in Table 2.

Property	**Available Values**
Control	OUTPUT_VOLTAGE, MANUAL
band_center	7200.0
band_width	120.0
time_delay	60.0
tap_pos_A	-16 to 16
tap_pos_B	-16 to 16
tap_pos_C	-16 to 16

Table 2: Properties available for control of *regulator_configuration* objects within GridLAB–D.

Regulator control has two *Control* modes:

- *OUTPUT_VOTLAGE* utilizes *band_center*, *band_width*, and *time_delay* to automatically control output voltage. The regulator uses tap positions to modify input voltage to try to reach the *band_center*. After each tap change, the regulator will not change again unless the voltage rises or falls by at least one–half of the *band_width* and, once it does, the regulator will wait for *time_delay* in seconds before changing.
- *MANUAL* uses only the *tap_pos_A*, *tap_pos_B*, and *tap_pos_C* to hold the regulator to the same setting the entire time.

3.2 Capacitor Settings

Capacitors add VARs or reactive power to the system. There is a *capacitor* object in GridLAB–D with numerous properties. Capacitor properties for this project are limited to those shown in Table 3.

Capacitors can be configured to run in three different *control* modes:

Property	Available Values
control	MANUAL, VOLT, VAR
switchA	OPEN, CLOSED
switchB	OPEN, CLOSED
switchC	OPEN, CLOSED
votlage_set_high	7740.0
voltage_set_low	7110.0
VAr_set_high	200.0 kVAr
VAr_set_low	-300.0 kVAr
time_delay	300.0
lockout_time	1

Table 3: Capacitor properties available for controlling capacitor banks in the project.

- **MANUAL** - capacitor remains in the state in which it is initially set which is indicated in *switchA*, *switchB*, and *switchC* properties.
- **VOLT** - capacitor reads the node voltage of the nearest upline node which is used along with the *voltage_set_high* and *voltage_set_low* properties to make a decision about when to switch on or off. Similar to voltage regulators, the capacitor waits for *time_delay* in seconds after the voltage has passed a voltage set point before operating.
- **VAR** - capacitors read the line reactive power of the nearest upline non-node which they use along with the *VAr_set_high* and *VAr_set_low* properties to make a decision about when to switch on or off. The capacitor waits for *time_delay* in seconds after passing the VAr set point before operating.

While it is possible to use a combination of VAR and VOLT, such a setting is out of the scope of this project.

3.3 File Configuration

The GridLAB–D files were copied three times in order to provide parallel run ability. Each copy relied on the same central model file to minimize changes required. Recorders were used to place all output data from simulations into the same set of results directories. Voltdump files were used at peak load times for Phase A, Phase B, and Phase C.

In addition to the utility–level problems found with the model and described in the introduction, the existing settings in the model used options not allowed for this project. These settings had to be modified prior to solving analysis.

- Capacitors banks *CapBank1* and *CapBank2* were using VARVOLT mode which is not allowed for this project.

- The *remote_sense* and *remote_sense_B* properties used for VAR and VOLT modes are only allowed to be set to nodes or links directly upline from capacitors. The remote sense properties for *CapBank2* were set to sense node and link points upline from *CapBank0*. This is true remote sensing and is out of the scope of this project.

3.4 Recorded Data

To determine how often the capacitors should operate, reactive power levels were recorded upline from each capacitor bank. To determine how often the regulators might operate, voltage was recorded at the nodes upline from each regulator.

In addition regulator tap changes and positions were recorded for each regulator and capacitor state was recorded for each capacitor.

To ensure ANSI Standards were being met, voltages of all meter nodes were recorded during peak load times for each phase.

3.5 Plots

The primary data representation was done with plots in Matlab. Plots allowed for quick visualization of kVAR for capacitors, voltage levels for regulators, and voltage profiles to see which element needed the adjustment for each area.

4 Analysis

The system was analyzed mostly during the winter day. The two summer days had very similar loads and, as shown in Figure 5, the winter load profile had far more demand. For this reason, the primary focus was on getting the system optimally configured for the winter load.

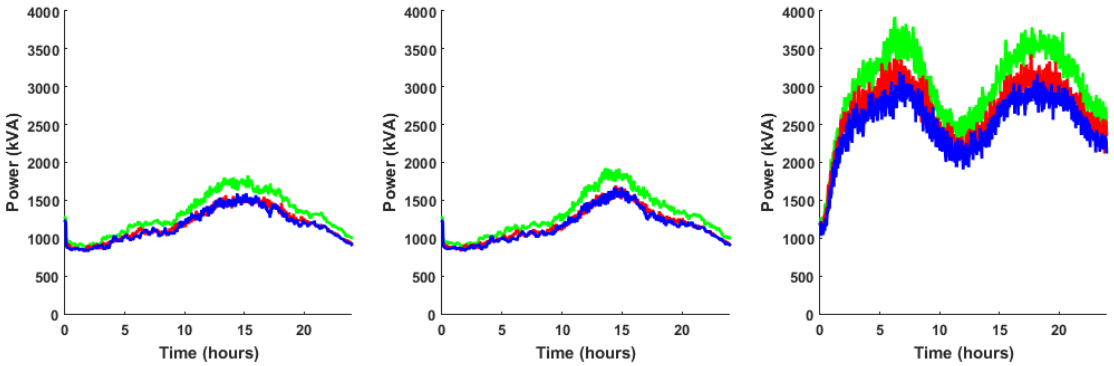

Figure 5: Power demand in kVA for each day. The two days in the summer are on the left and center while the single day in the winter is on the right.

To begin work analyzing the model, all invalid settings were eliminated. Then regulator and capacitor names were matched to the regulators and capacitors on the map shown in Figure 4 so that the effects of regulators and capacitors on each other could be better predicted during further changes to the model.

To accomplish this, all capacitors were set to MANUAL and OPEN and all regulators were set to MANUAL with taps all at 0. The resulting voltages at each plot for this are shown in Figure 6.

Using a voltage dump from the peak voltage time for Phase A, 6:02 AM during the winter day, a voltage profile can be produced which more easily shows the relationship between the two legs of the feeder, as shown in Figure 7. Until the line splits, the elements go FEEDER_REG, CapBank2, CapBank1. After the split, on the upper leg of the feeder, we have VREG3, CapBank0, VREG2 and on the lower leg, we have VREG4 and CapBank3. This relationship is why the voltage profile is split into two plots.

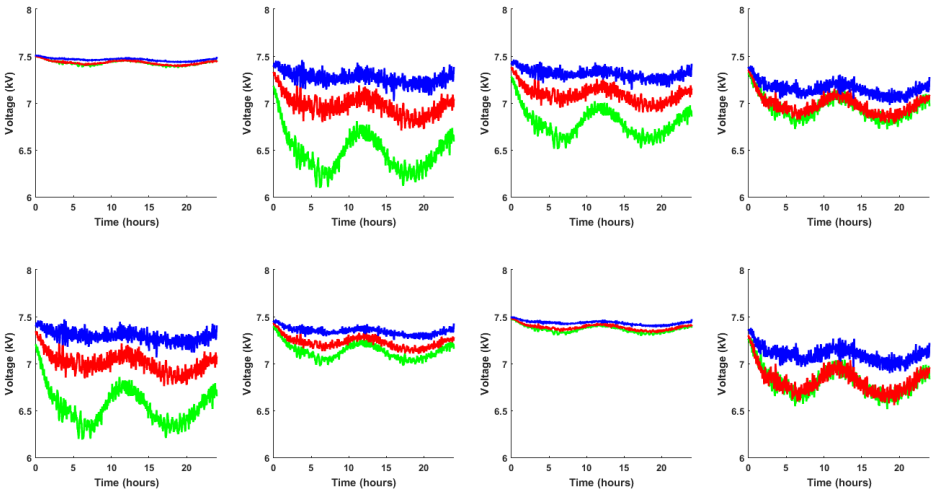

Figure 6: The voltages of each regulator and capacitor throughout the day. The top row of plots is voltage for the regulators in order, FEEDER_REG, VREG2, VREG3, VREG4 while the bottom row of plots is capacitors in order, CapBank0, CapBank1, CapBank2, CapBank3.

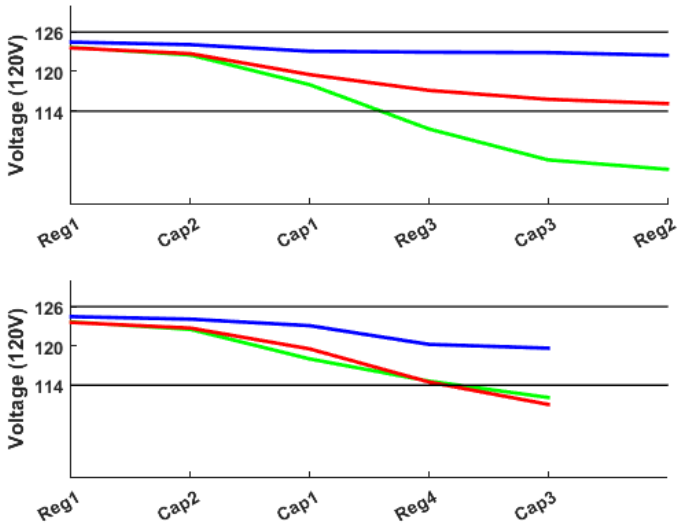

Figure 7: The voltage profile when all regulators and capacitors are turned off. There are two plots because the feeder splits into two legs.

4.1 Capacitor Adjustments

Starting with the base configuration of all capacitors off, the kVAR values just above each capacitor can be seen in Figure 8.

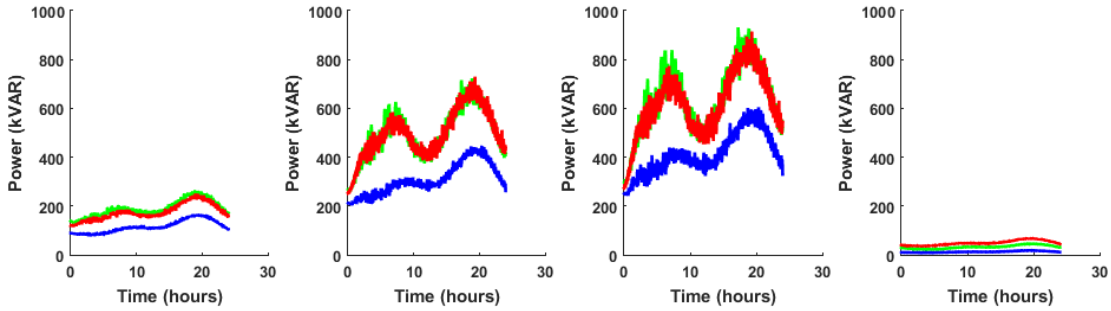

Figure 8: Reactive power plots for power just upline from capacitor banks, in order from left to right, for CapBank0, CapBank1, CapBank2, CapBank3.

From Figure 8, it is clear that the reactive power levels above CapBank1 and CapBank2 are far too high. The first three capacitor banks were set in the following manner:

- CapBank0 was set to a control mode of VAR with a high value of 200 kVAR and a low value of -300 kVAR. This should reduce the reactive power seen in the evening.
- CapBank1 was set to a control mode of MANUAL with all three phases closed. This should reduce the shown reactive power in the plot in Figure 8 down by 3 kVAR per phase, something that it appears is needed.
- CapBank2 was set to a control mode of VAR with a high value of 500 kVAR and a low value of 150 kVAR. The intent is to reduce the peak reactive power.

After making the changes and rerunning the simulation, the new reactive power levels can be seen in Figure 9. The changes had the desired effect, bringing the reactive power levels down sometimes even driving them negative or leading. An unintended consequence can be seen in the plot for CapBank2 where there is a small spike downward. This is due to timing of the capacitor banks lining up too evenly. A staggered time delay was used in later changes. Lower reactive power levels mean a power factor closer to unity which in turn means lower cost of generation for power utilities.

The changes to the capacitor banks was able to raise the voltage for some parts of the model, as shown in Figure 9. Unfortunately, a large number of houses retained voltage levels below the ANSI voltage minimum. Of interesting note is how well Phase C, in blue in all plots, is faring throughout the analysis. Phase C has far less voltage drop than the other two phases.

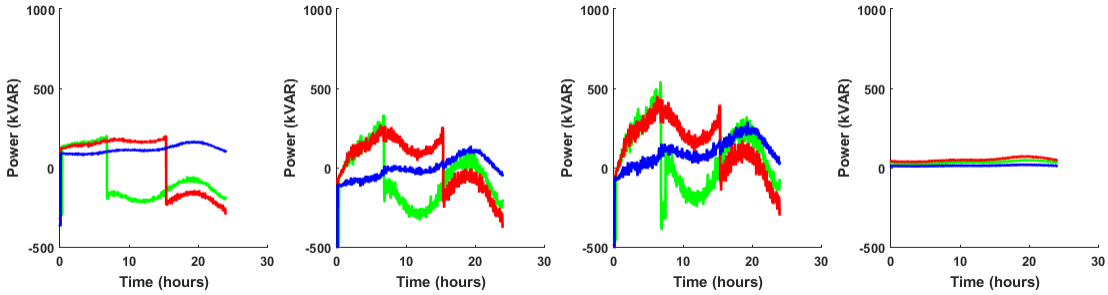

Figure 9: Reactive power plots for power just upline from capacitor banks. This is after CapBank0, CapBank1, and CapBank2 have been enabled.

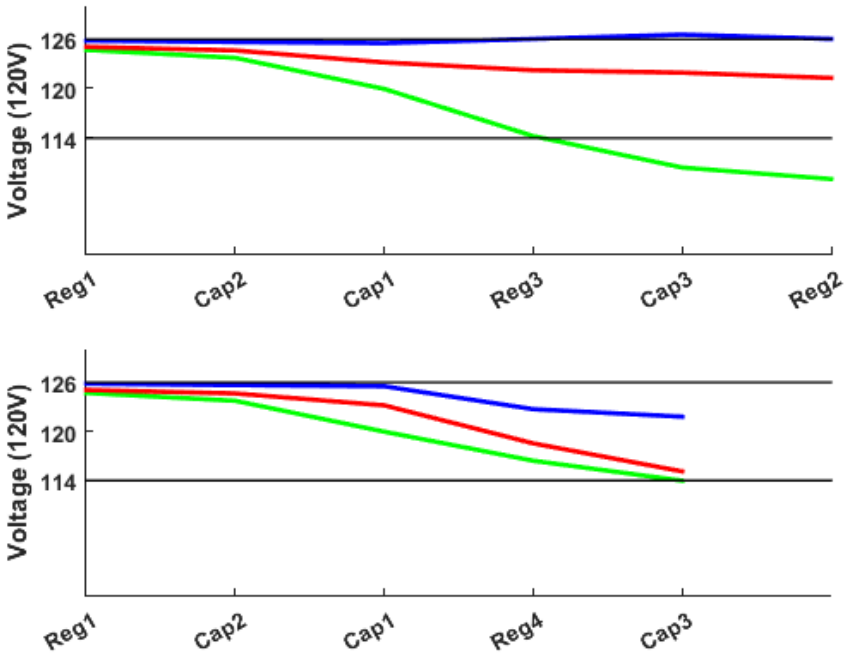

Figure 10: The voltage profile seen after CapBank0, CapBank1, and CapBank2 were enabled.

4.2 Regulator Adjustments

The most instructive plot for adjusting regulator settings is in Figure 3 in the introduction. In this plot, it is clear that regulators on this system need a time delay at a minimal setting of 5 to 10 minutes (300 to 600 seconds).

Providing longer time delays, the regulator tap change counts went down significantly, as shown in Figure 11.

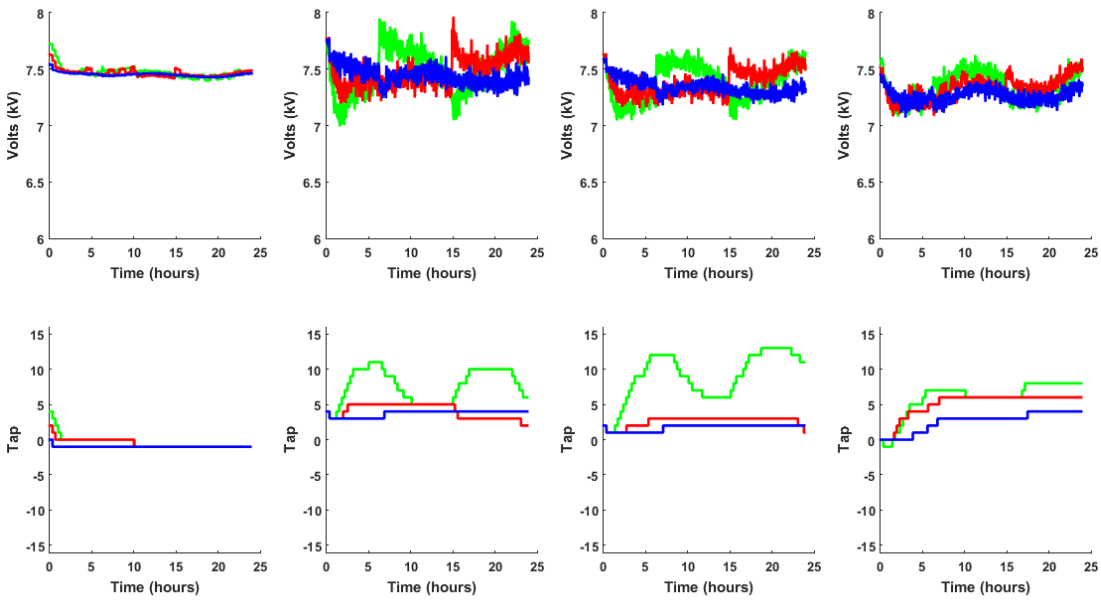

Figure 11: Voltages just upline from regulators and the tap changes that each regulator made in response to the voltage.

The voltage profile after regulator adjustments were made is shown in Figure 12. Unfortunately, VREG3 is still landing below the ANSI Voltage Minimum and leads directly to ANSI Voltage Standard violations for all houses downline from it.

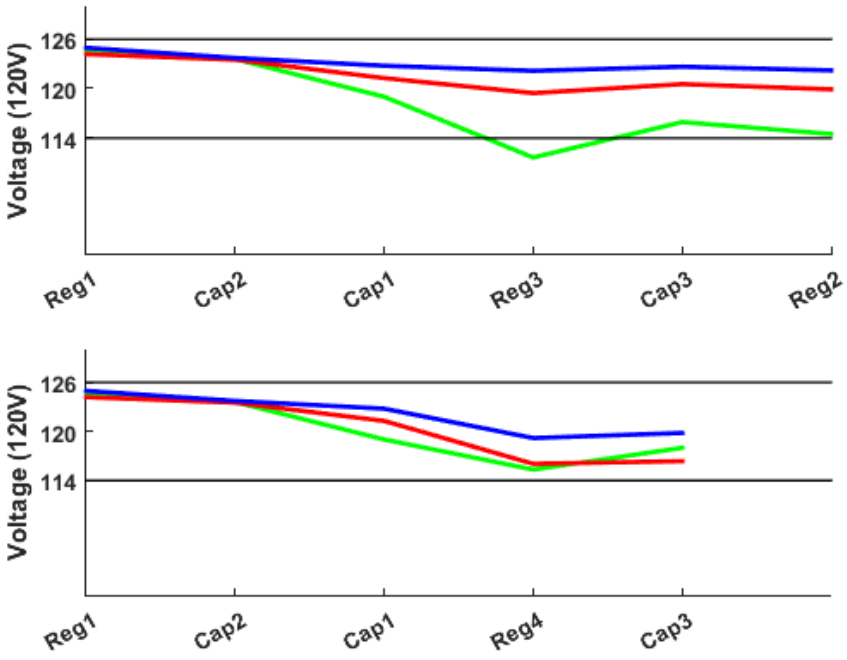

Figure 12: Voltage profile for the two legs of the feeder showing marked improvement of voltages.

5 Conclusions

Gaining complete stability of the IEEE 8500 Node Test Feeder has been unattainable after more than two dozen simulations with adjustments each time. It is clear from the description documents that the system is heavily loaded down for the static version of analysis. The peak load during the winter causes ANSI voltage standard issues at some nodes and regulator and capacitor control challenges throughout the system.

5.1 Recommendations

It does seem that with a little more tweaking, the remaining few customers who experience voltages at 106% which is just 1% over the ANSI Voltage Standard maximum could be addressed. Even with this knowledge, the system will have been designed for a very specific set of load profiles and load profiles grow almost every year.

If this were a real utility network, a few choice changes could help mitigate the need for introduction of more equipment.

- **Load Balance:** As was visible in numerous figures throughout this report, the Phase A load exceeds the Phase B and Phase C loads every day and almost at every time. The utility should definitely do a load balance study. Perhaps some of the Phase A load can be served by Phase B or Phase C instead. Balancing the load might be enough to fix the problems.
- **Remote Sensing:** Although unavailable for this project, remote sensing could eliminate the need for additional equipment. However, remote sensing itself takes equipment so that might not be as effective as an extra regulator.

5.2 Modeling Recommendations

Determining valid data from a purely text based model is exceedingly difficult. The Load Balance study recommended would be difficult to complete without knowing geospatial information about where the different lines could be changed to tap from other phases.

A geospatial model inside a clean graphical user interface (GUI) would allow the utility to easily see which customers are having voltage problems during peak load. Placement of new capacitors or regulators to mitigate the problem would then be far easier to discern.

References

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